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Title: Fast Hybrid and Monolithic CMOS Imagers in Multi-Frame Radiography

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Fast Hybrid and Monolithic CMOS Imagers in Multi-Frame Radiography

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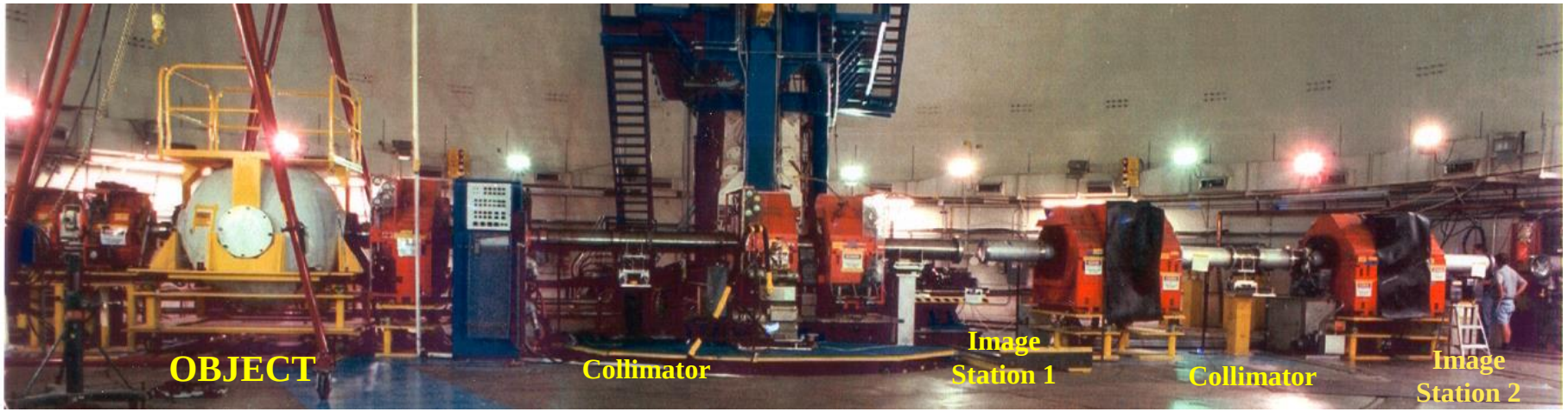
LA-UR-14-

Talk Overview

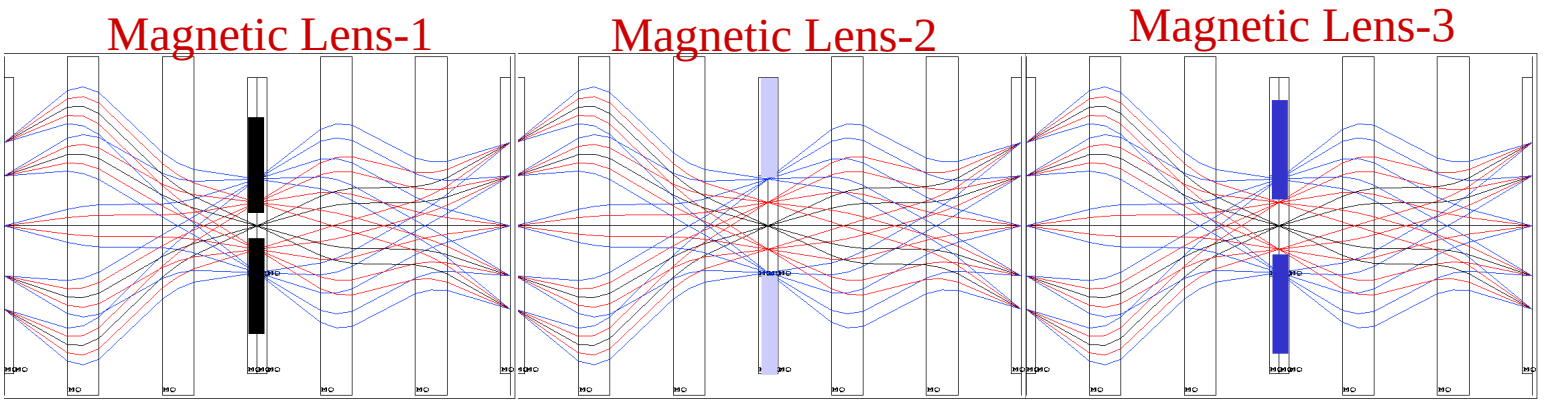
- Multi-frame proton radiography (pRAD)
- Two generations of hybrid imagers at Rockwell Scientific (now Teledyne Imaging Sensors)
- Initial data with new 1.2Mpx hybrid chip
- Monolithic CMOS Imagers
- Other CMOS visible camera options

800 MeV Proton Radiography Facility at LANSCE

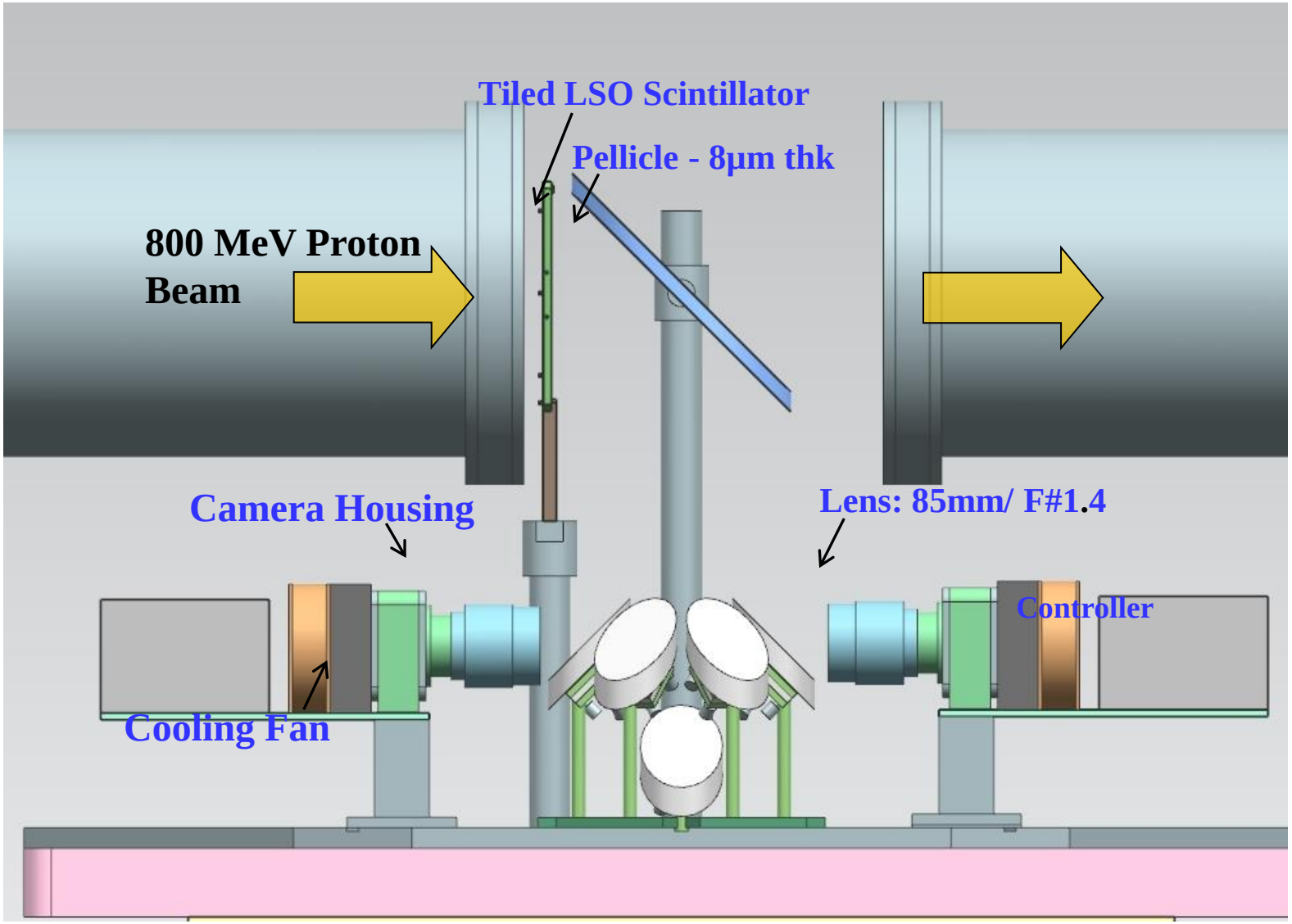


Multiple (1-to-1000's) beam pulses: ~50ns wide; spacing 5ns-to-ms

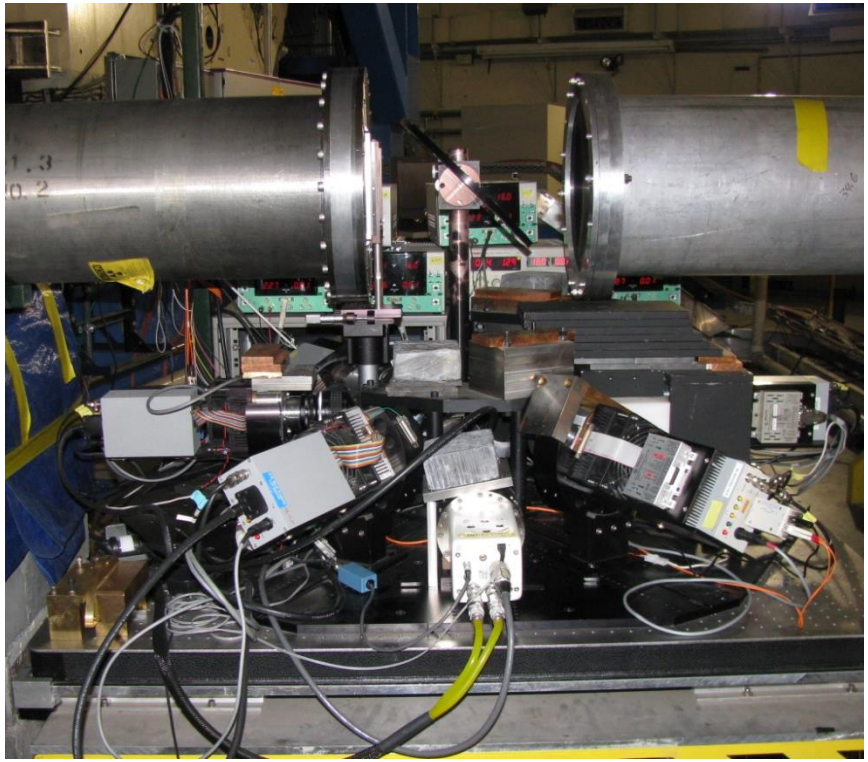
Beam dynamics, ray trace:

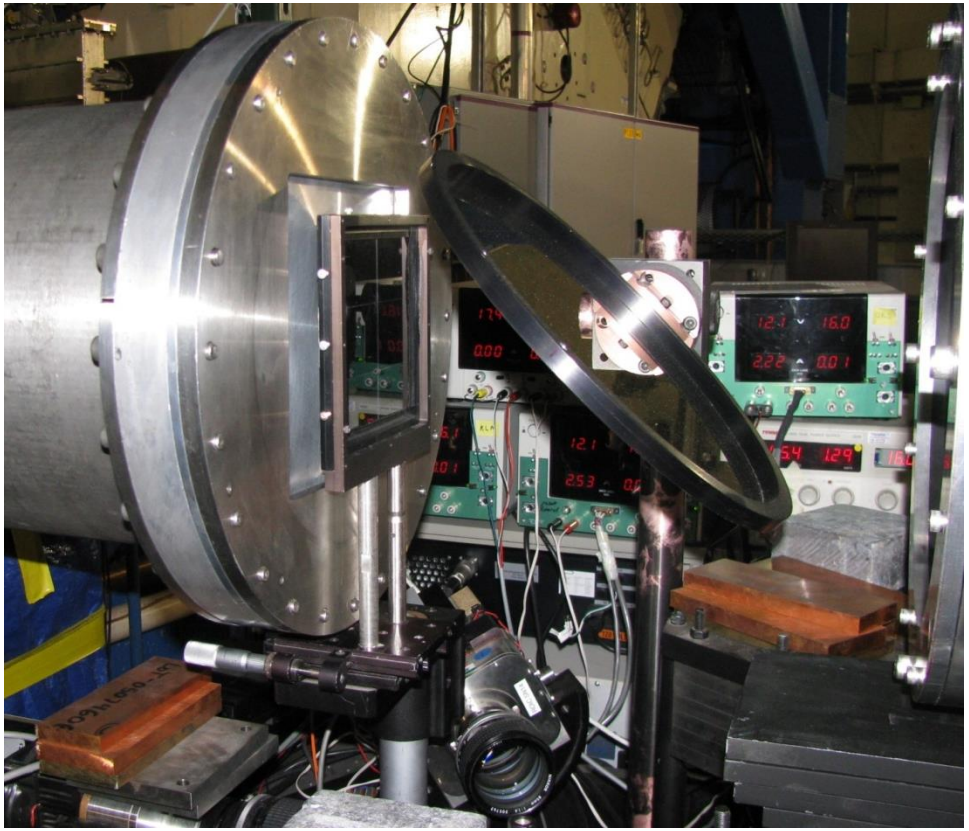


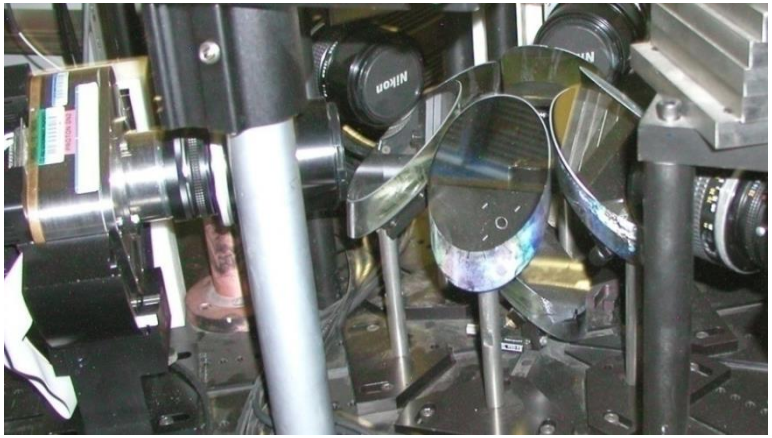
Camera installation for experiments



Scintillator and Cameras at Image Stn1





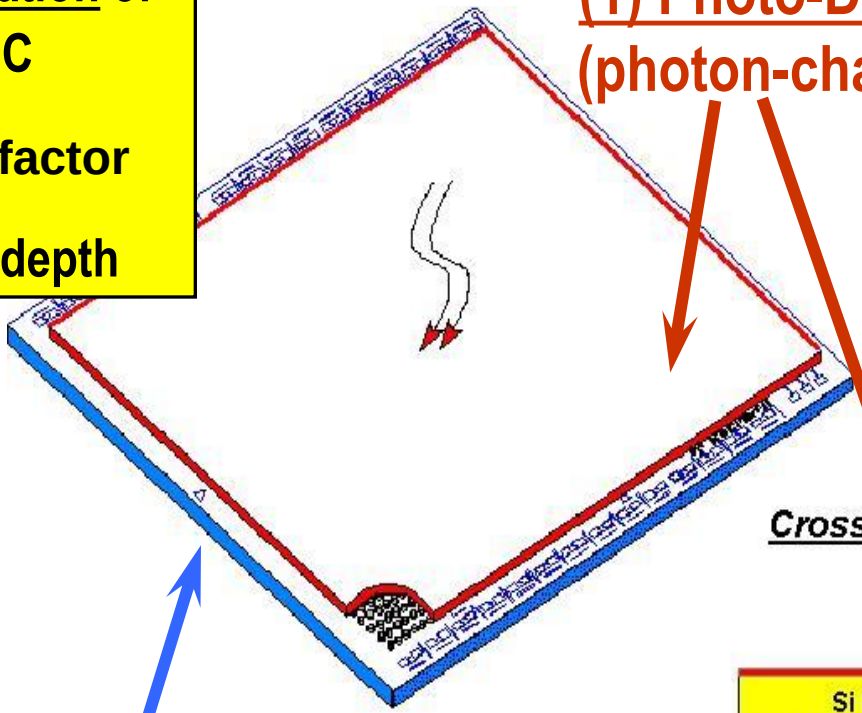


Compact mirror and camera packing

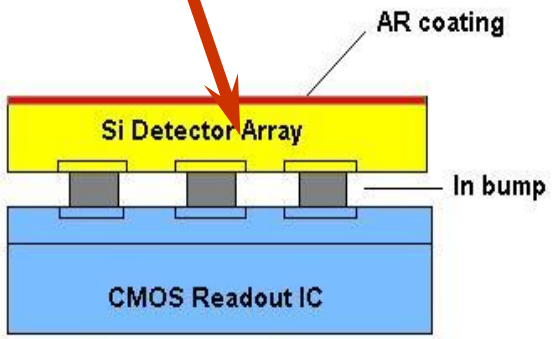
Imager as Two-Component Hybrid Focal Plane Array (FPA)

- Independent optimization of detector and readout IC
- ~100% optical fill factor
- Arbitrarily large well depth

(1) Photo-Diode Pixel Array (photon-charge conversion)



(2) CMOS Readout IC (ROIC): charge-to-voltage conversion, signal storage & processing, logic and A/D conversion; *System on Chip (SoC): photons-to-bits*



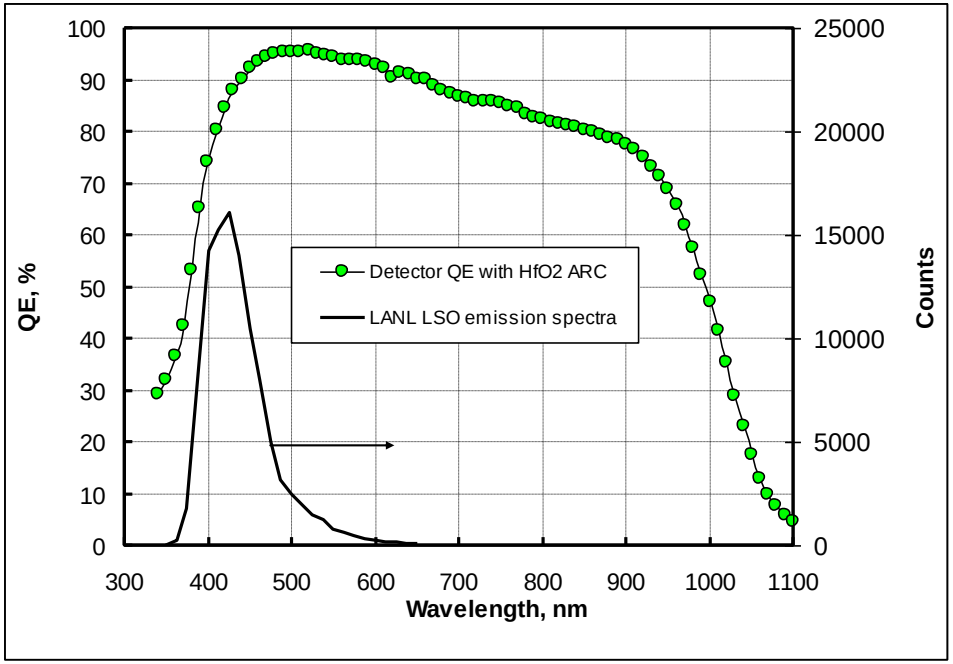
Each pixel in PD Sensor Array bump bonded (dia.< 10μm) to corresponding pixel in ROIC

3-frame “pRAD-1” Hybrid Burst Mode Imager

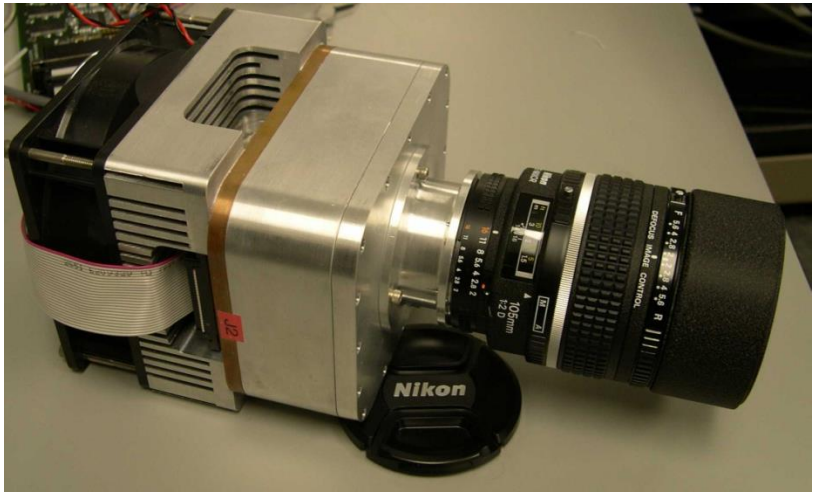
- Number of frames: 3
- Min. shutter time: 180 ns (40ns)
- Inter-frame time: 350ns (250 ns)
- Array Size: 720×720
- Eff. Dynamic Range: 10.5-bit (12-bit ADC)
- Read Noise: 150 e^-
- Well depth : ~180 ke^-
- QE 84% (at 415nm)
- Pixel size: 26 µm
- Chip size: 21.4mm×21.9mm

- CMOS technology: standard UMC 250 nm

Rockwell Scientific pRAD Camera



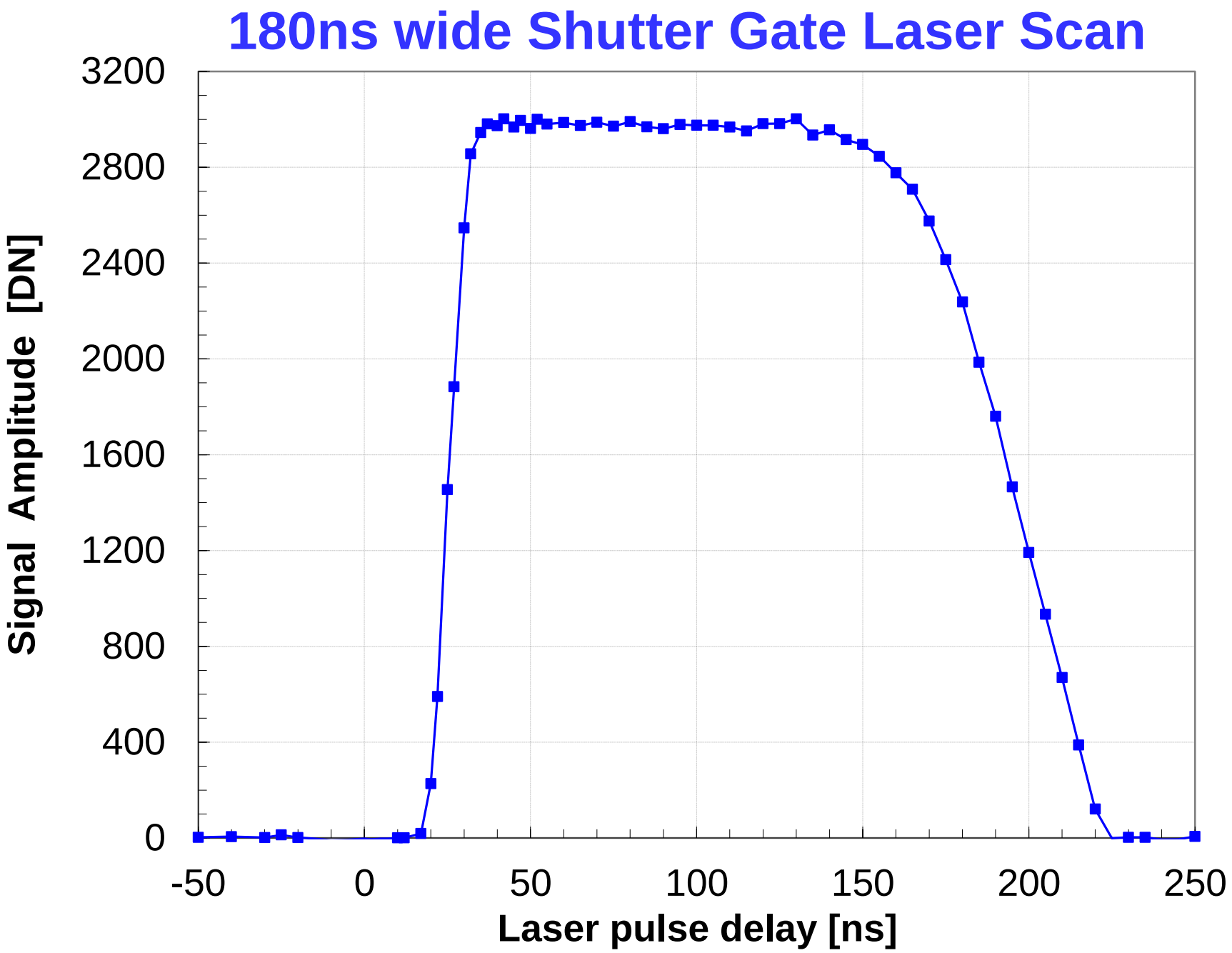
Excellent QE, good match to LSO-scintillator emission spectrum



Compact package

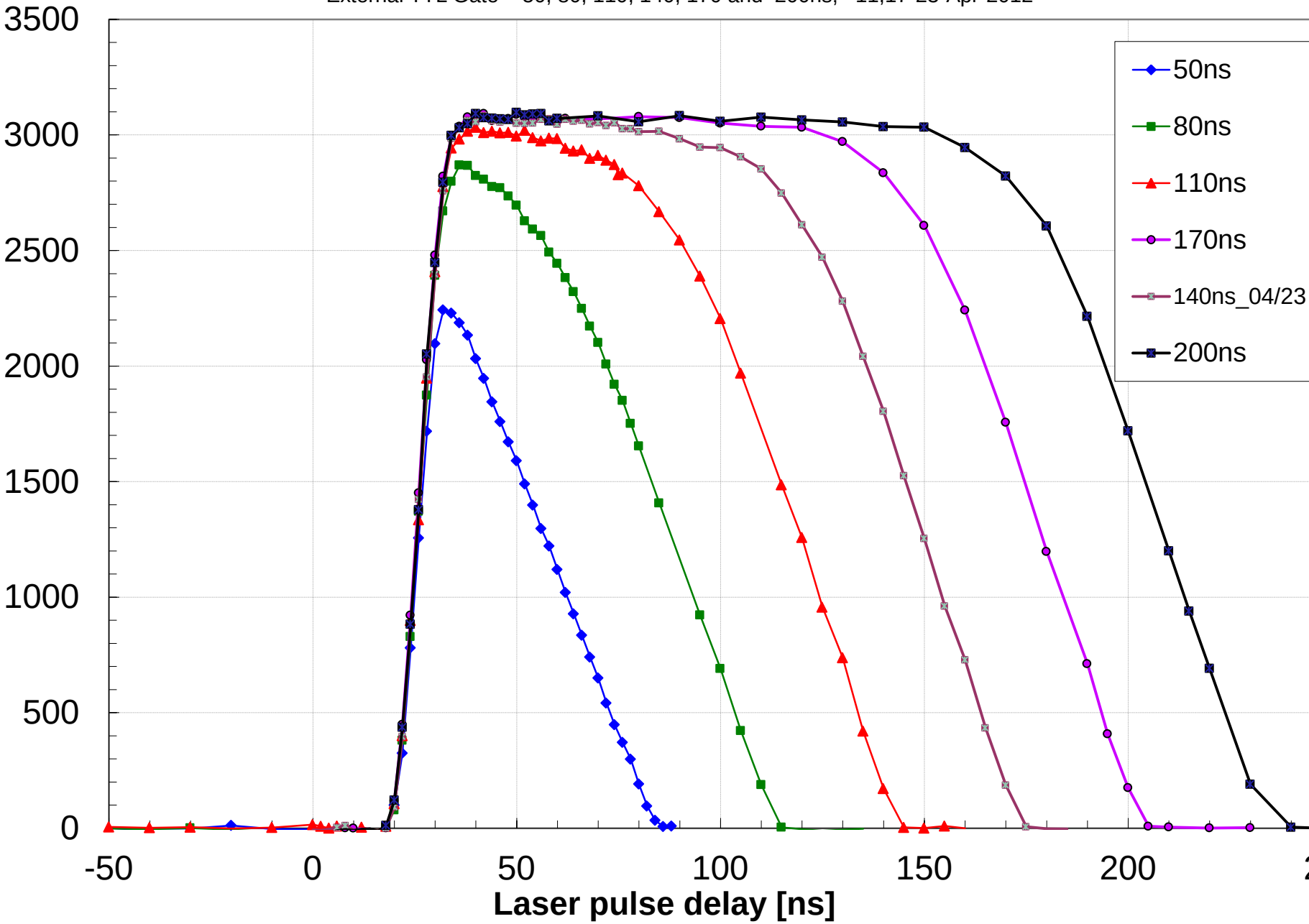
Fast electronic shutter with min. exposure of 150ns, 250 ns inter-frame time.

→ **Limited number of frames (3) and resolution (720×720 px)**

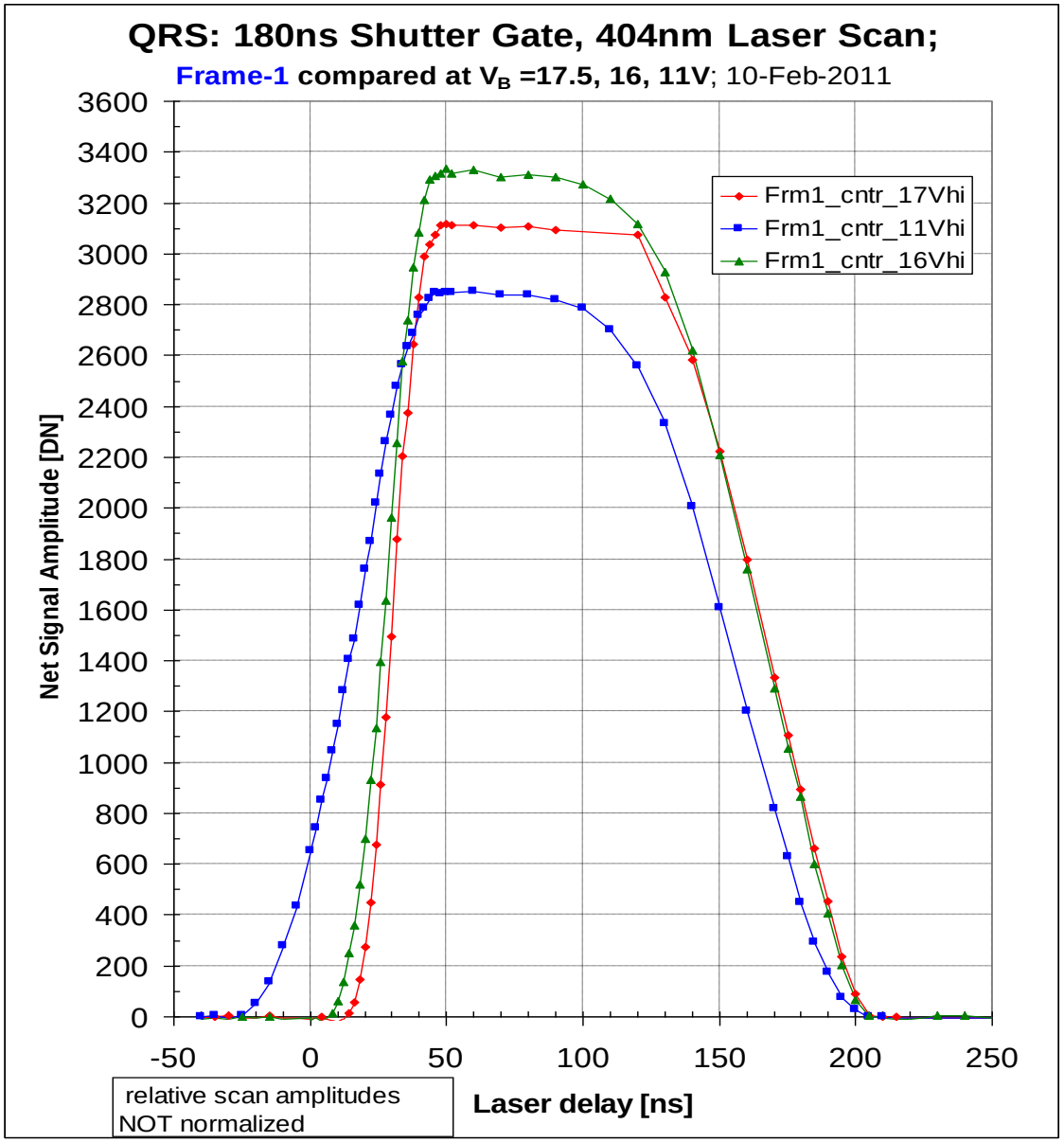

180ns wide Shutter Gate Laser Scan
Signal Amplitude [DN]
3200
2800
2400
2000
1600
1200
800
400
0
-50
0
50
100
150
200
250
Laser pulse delay [ns]

Evolution of Effective Shutter Gate; Frame2

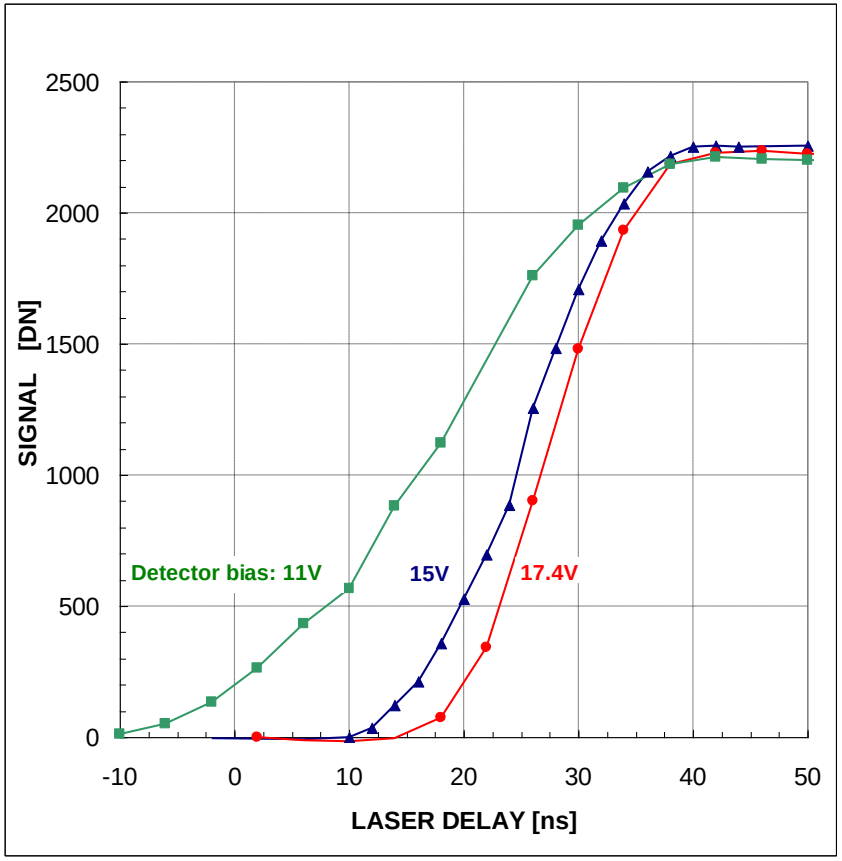
NSTec: V_B=26V, EAF7, t=1°C; 404nm 70ps Laser Scan; All at (295,326)
External TTL Gate = 50, 80, 110, 140, 170 and 200ns; 11,17-23-Apr-2012



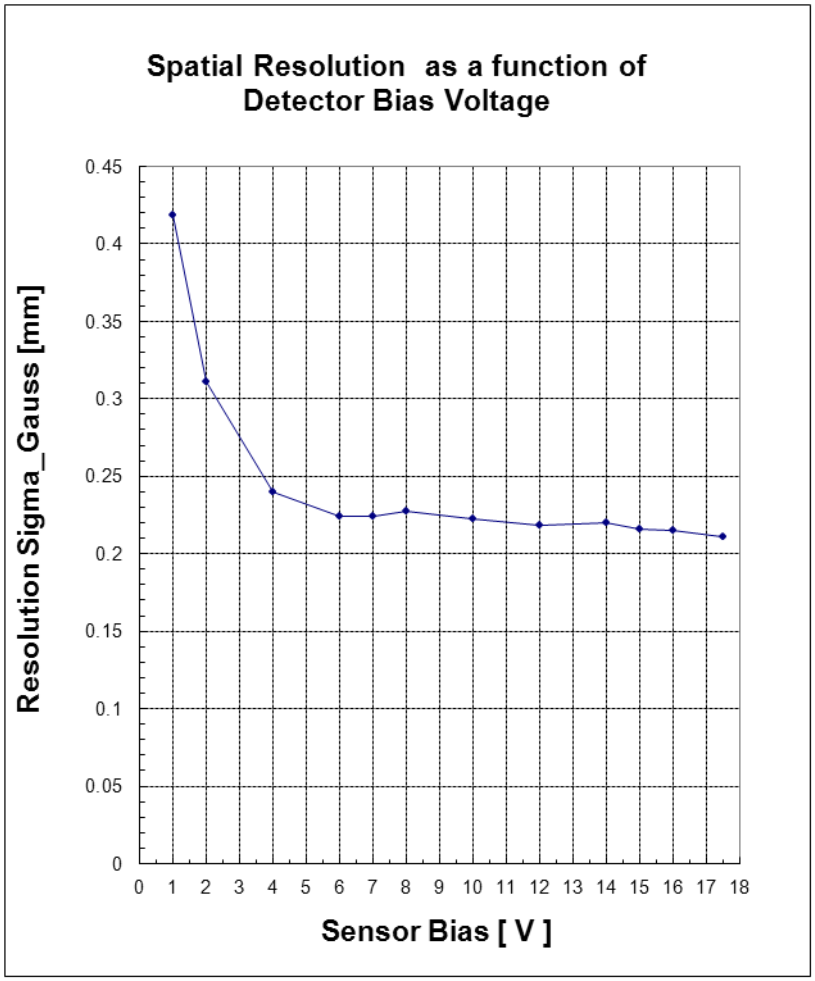
Shutter gate response to photo-sensor bias



Leading-edge Dependence of Shutter Gate on Photo-Detector Bias Voltage

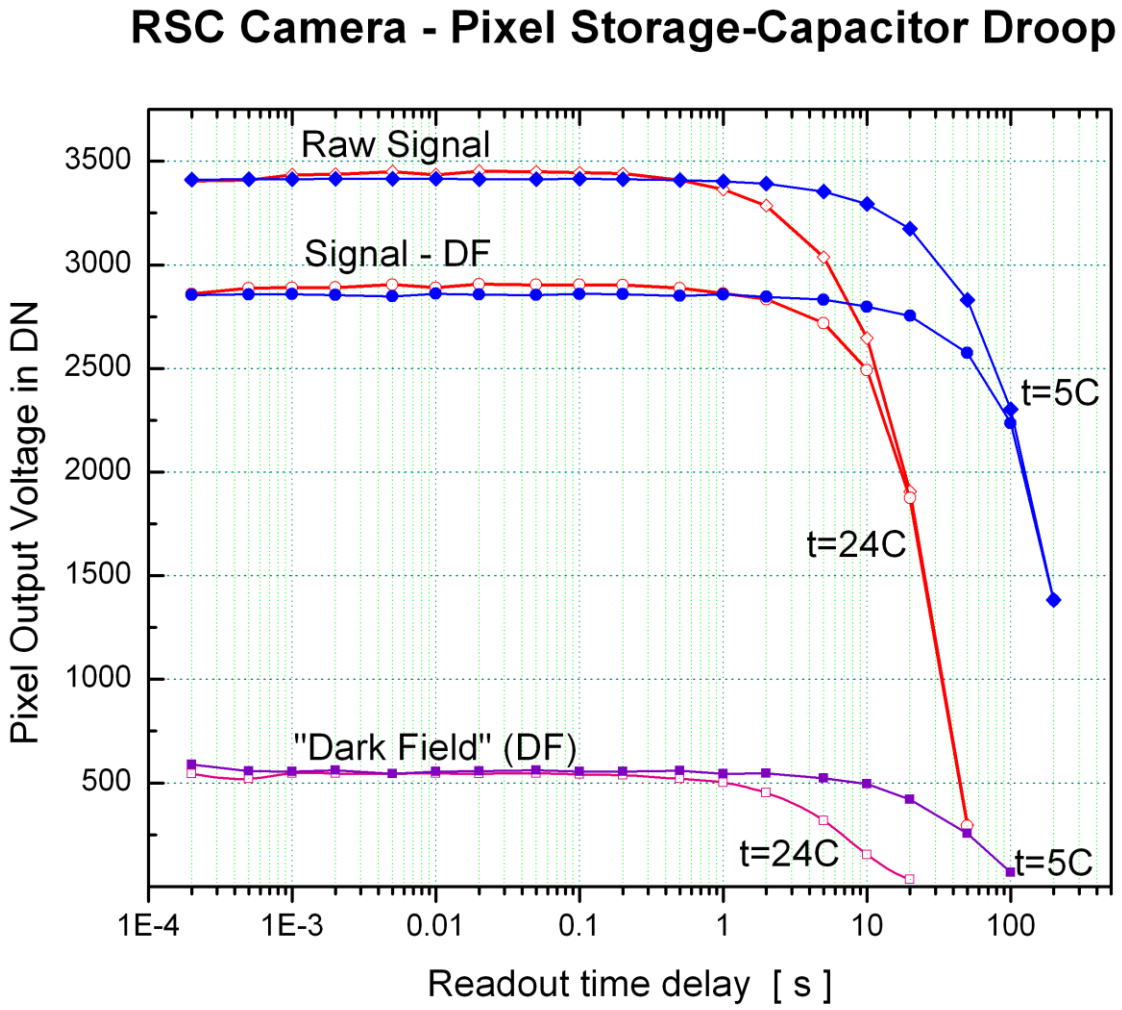


The effective "rising edge" of shutter is longer than the expected carrier collection time (16ns, 11.8 ns and 10.1 ns at 11 V, 15 V, and 17.5 V bias). Front-end electronic is contributing as well.



However, the detector bias has remarkably little effect on the spatial resolution, as long as $V_{\text{full depletion}} \leq V_{\text{bias}}$

In-Pixel Storage Signal Leakage



Leakage current in the switching FET's and possibly in the oxide - limits the length of time charge storage to 0.5sec at room temperature to ~3sec at +5°C.

Full FPA array read-out completed in 3×26ms = 78ms

3-Frame Rockwell Imager issues and limitations

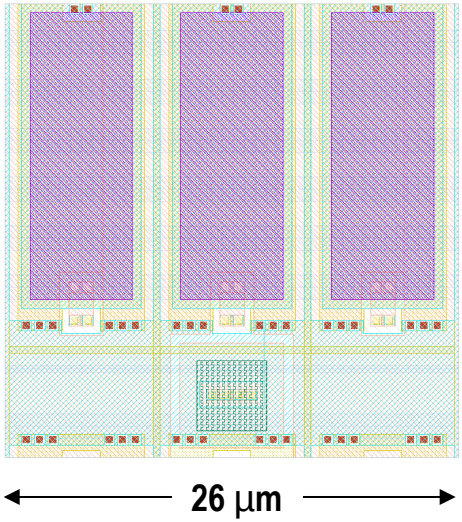
- Pixel count 0.5Mpx (720×720 px); FPA's are 2-side buttable
- 7 cameras × 3-frames (21 frames at IL1)
- CMOS readout integrated chip (ROIC)
  - large noise (~ 150e^- at room temperature)
  - dark-field non-uniformity → large offset, cuts into DR
  - DF frame-to-frame fluctuations (row dependent)
    fix: 2 strips of dark/ reference pixels added
- Si photo-sensor large leakage current up to 300 nA/cm^2 @RT vs. 10nA/cm^2 spec'ed (new detectors i < 5 nA/cm^2)
- Indium bump-bonding

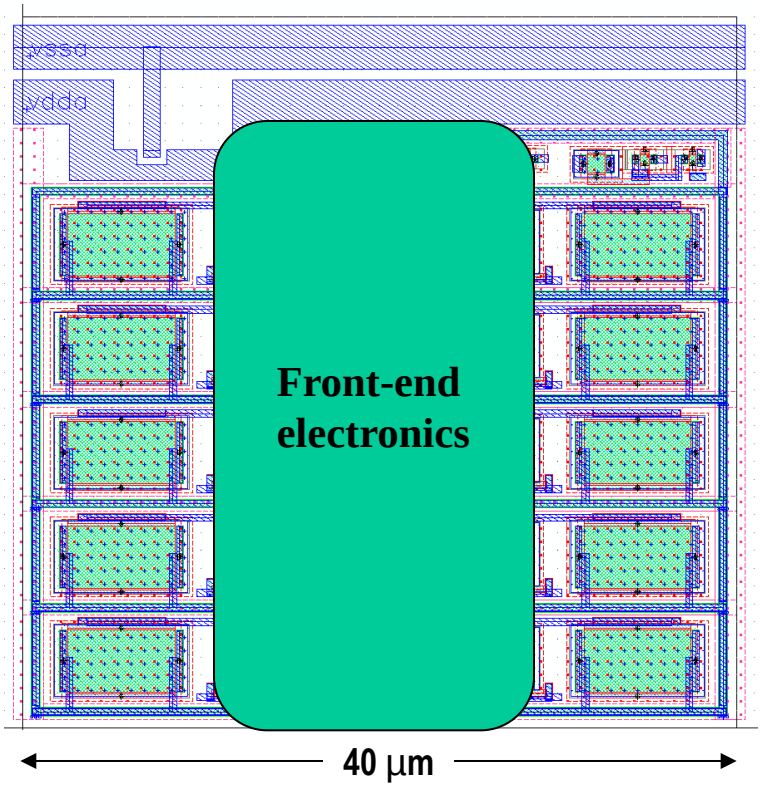
  - expensive

  - bump bonding affects yield and operability

Pixel layout: 1st vs 2nd gen. pRAD Imager

(3-frame vs.10-frame ROIC)



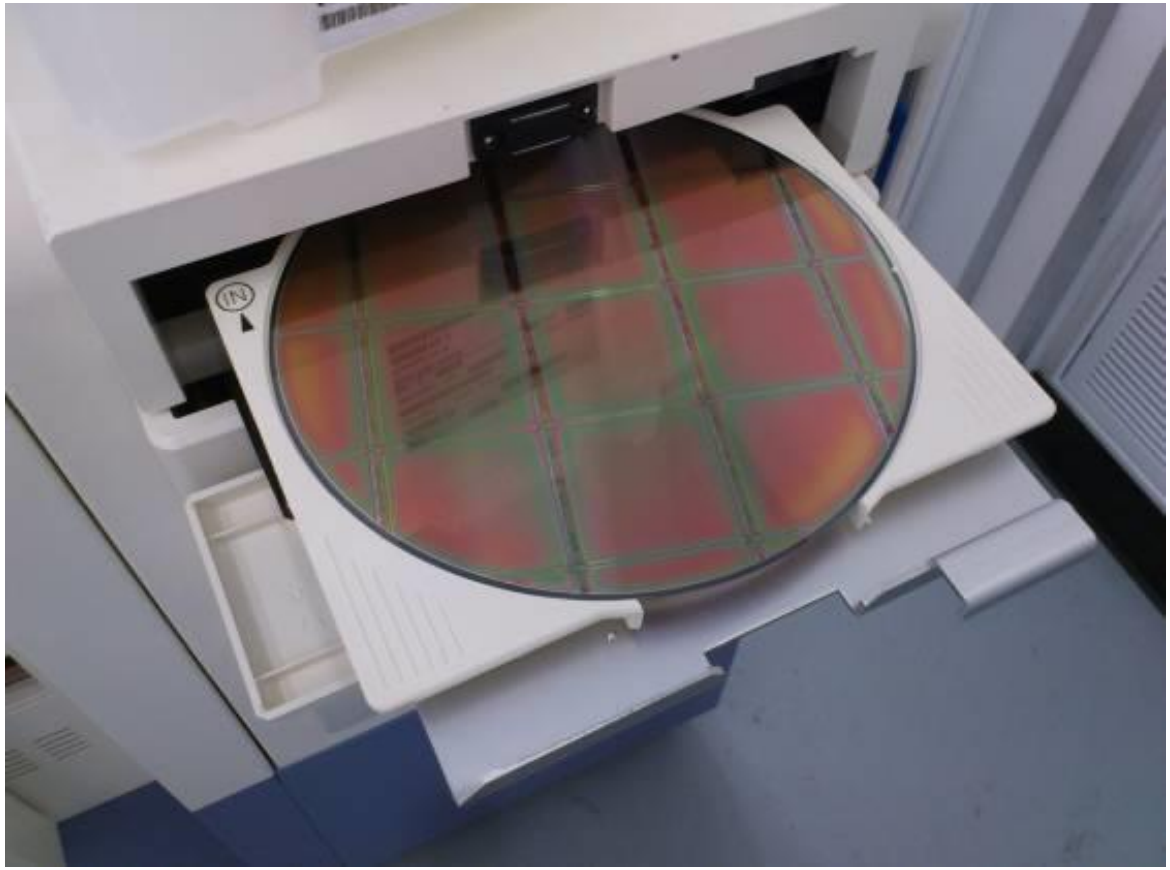


Original pRAD-1 26µm pixel. 40µm pixel, in 180 nm CMOS process (higher capacitance/µm^2) allows to pack 10 signal storage capacitors per pixel (storage for 10 frames). → Large area IC chip = 47 × 50 mm^2, needs "CMOS sub-field reticle stitching." Higher cost and *lower yield*.

1st and 2nd Gen pRAD CMOS Hybrid Imagers

Design Parameter	pRAD-1 Imager	2nd Generation pRAD-2 Imager
Minimum integration time (Global shutter)	150 ns	50ns
Nominal min. inter-frame time	350 ns	250 ns
Effective Dynamic Range	10.5 bits	~12 bits (13-bit ADC)
Read noise	150 e-	~ 45 (65) e-
Saturation charge/ Well depth	180 ke-	~ 240 ke-
Number of frames	3	10
Optical Fill Factor	~100 %	~86 %
Sensor QE @ 415 nm (*FF)	84%	68%
Pixel pitch	26 μm	40 μm
Imaging array pixel count	720×720 px	1100×1100 pixels
Sensor Imaging area	19×19 mm^2	44×44 mm^2

Wafer w/ new pRAD-2 ROIC Chips

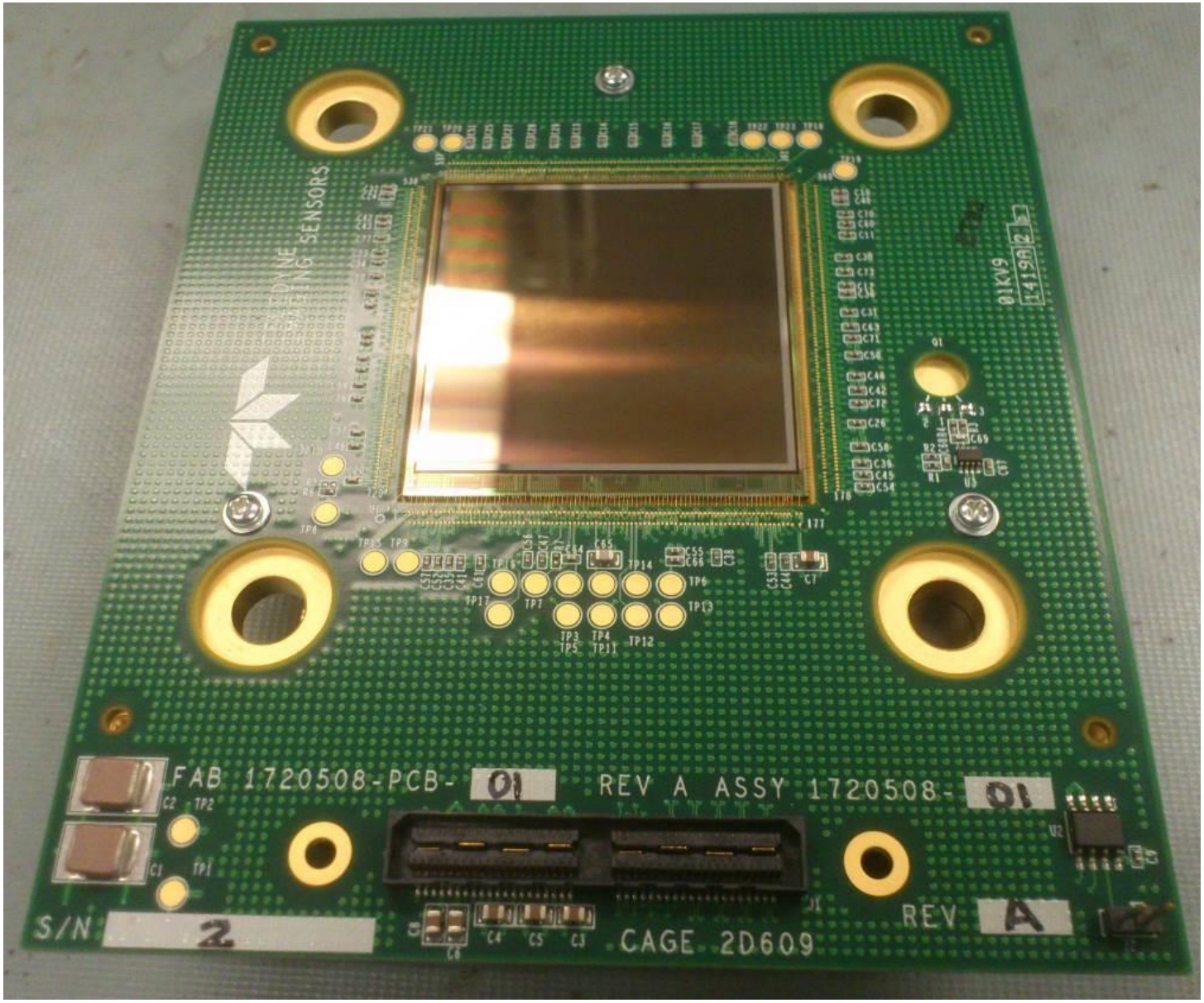


A 200mm diameter CMOS wafer with seven pRAD-2 ROIC's at a probe station

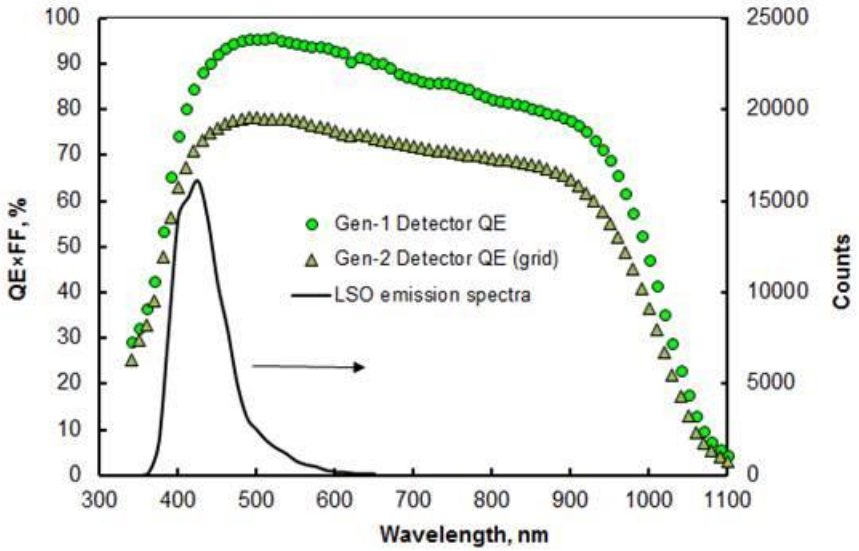
Signal crosstalk issues in the first CMOS fabrication required re-design, and an additional 10-wafer fab. run.

Large chip area
=> low CMOS yield

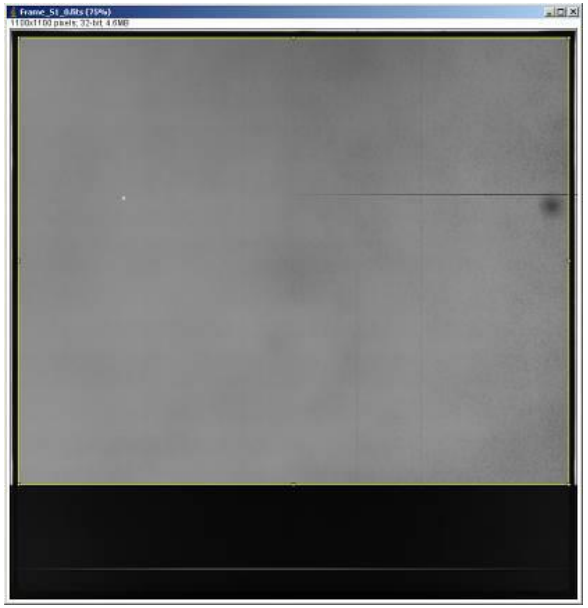
pRAD-2 hybrid mounted on Moly base-plate



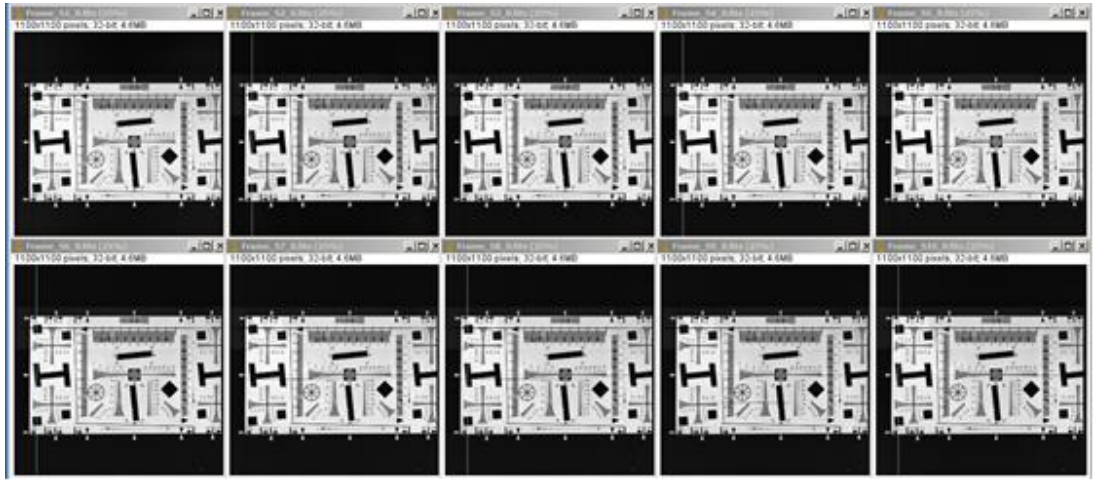
Two functional pRAD-2 FPA's fabricated



QE affected by AR coating and
3μm-wide Alu grid on top of photo-sensor

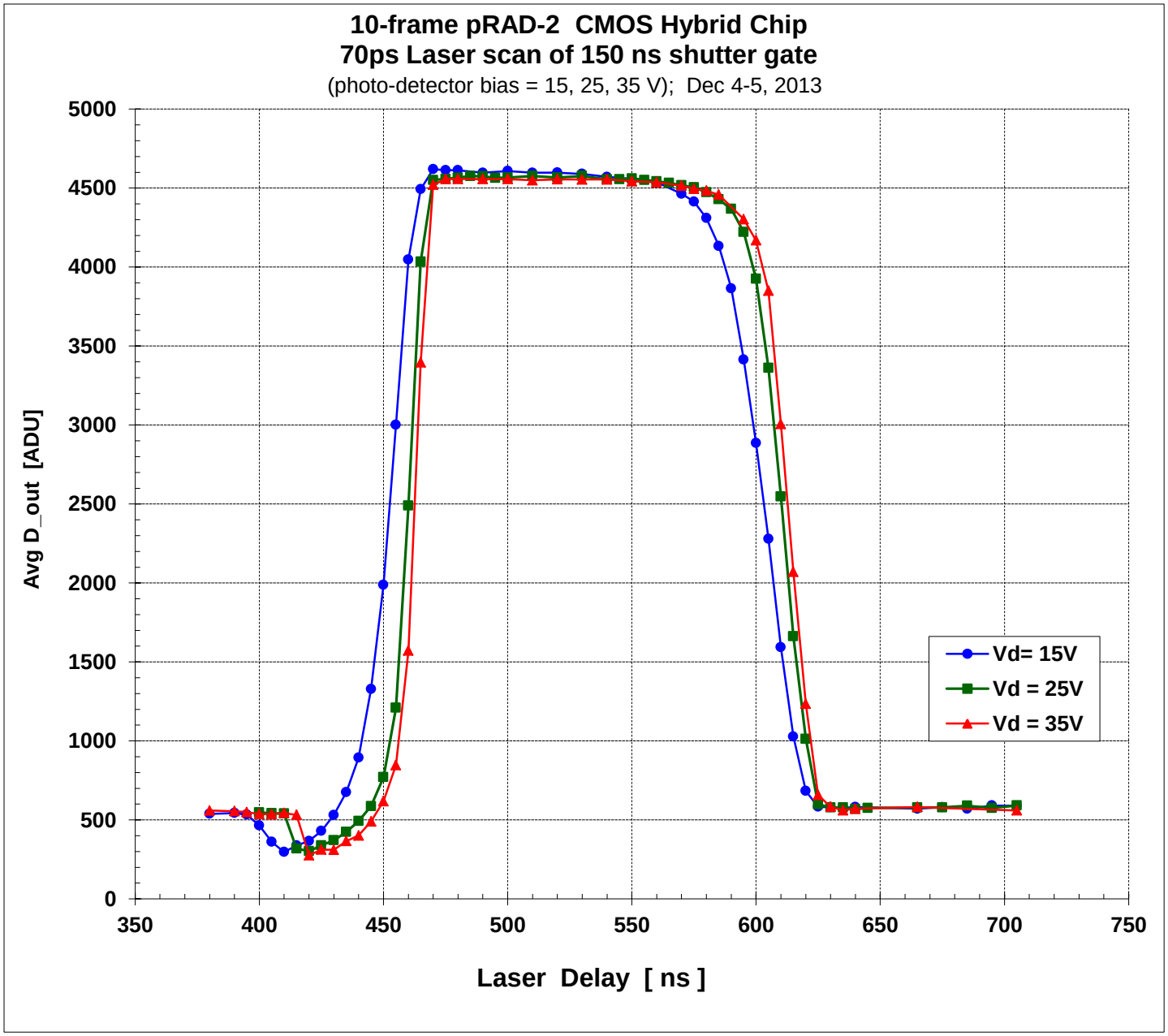


In one FPA 20% of sensitive area damaged during bump bonding/ mounting



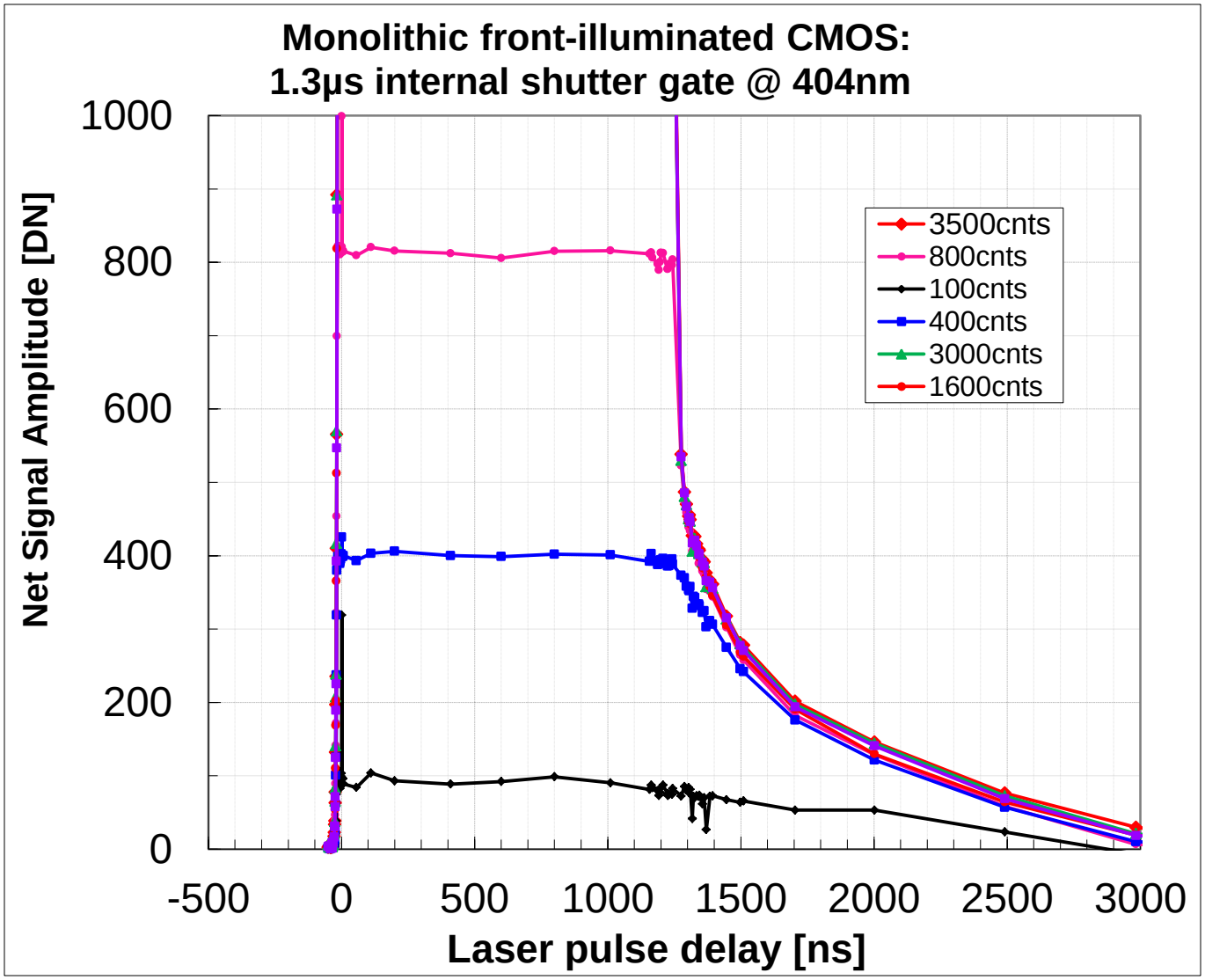
10 sequential frame capture;
proton-beam tests this Fall

70ps Laser Scan of 150 ns wide Shutter Gate



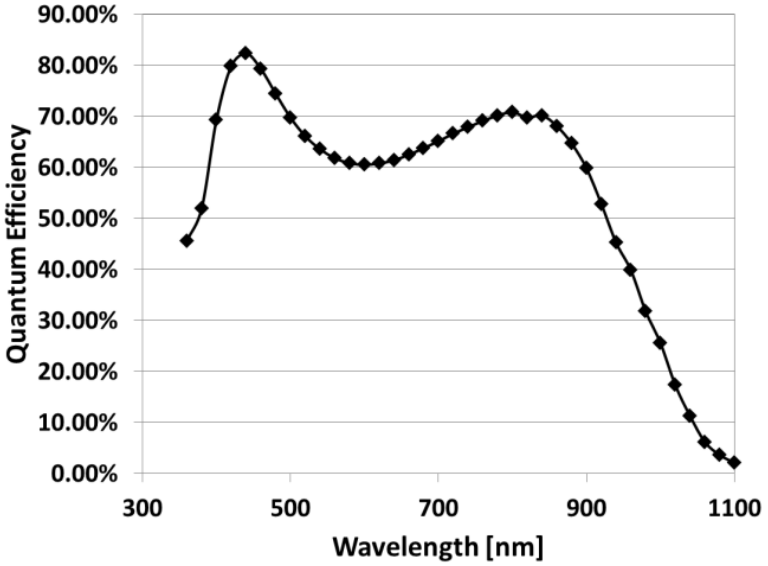
A commercial front-illuminated fast CMOS camera

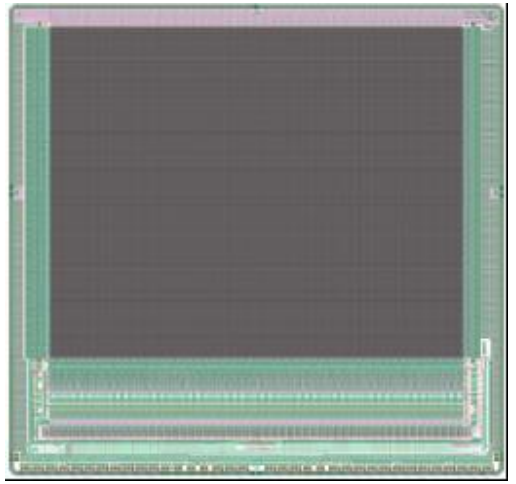
- Low QE – optical fill-factor & no AR
- Mpx resltn, but small pixels
- Shutter gate width > 1 µs
- Dark field fluctuations
- Extinction ratio issues
- Ghost/ latent images



A high-QE alternative to hybrid architecture: Fully-Depleted Backside-Illuminated (BSI) Monolithic CMOS Imager

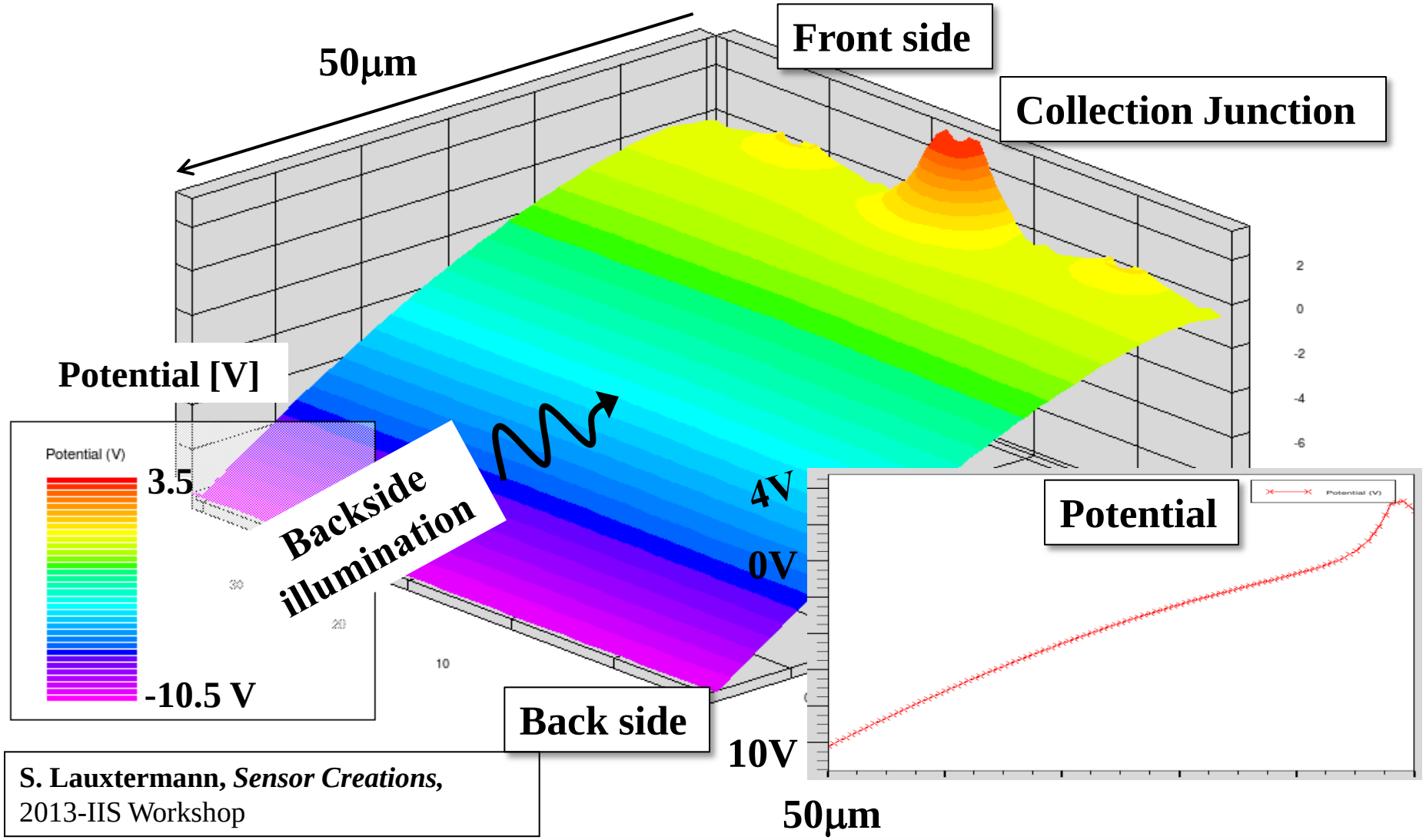
- Intevac, STMicroelectronics, Sensor Creations, CMOSIS, Samsung Electronics,…
- Photo-detector and signal processing CMOS electronics integrated on a high-resistivity silicon chip (**50** to 200μm thk).
- ***Sensor Creations:*** VGA format, 15 μm pixel, **100ns** to 30ms shutter, QE~75 - 80%, noise= 10e-; collect e- not holes; Camera available this Fall
  (S. Lauxtermann - 2013-IIS Workshop)





12mm×12mm *SC* BSI chip

Potential Distribution Throughout BSI Detector Volume



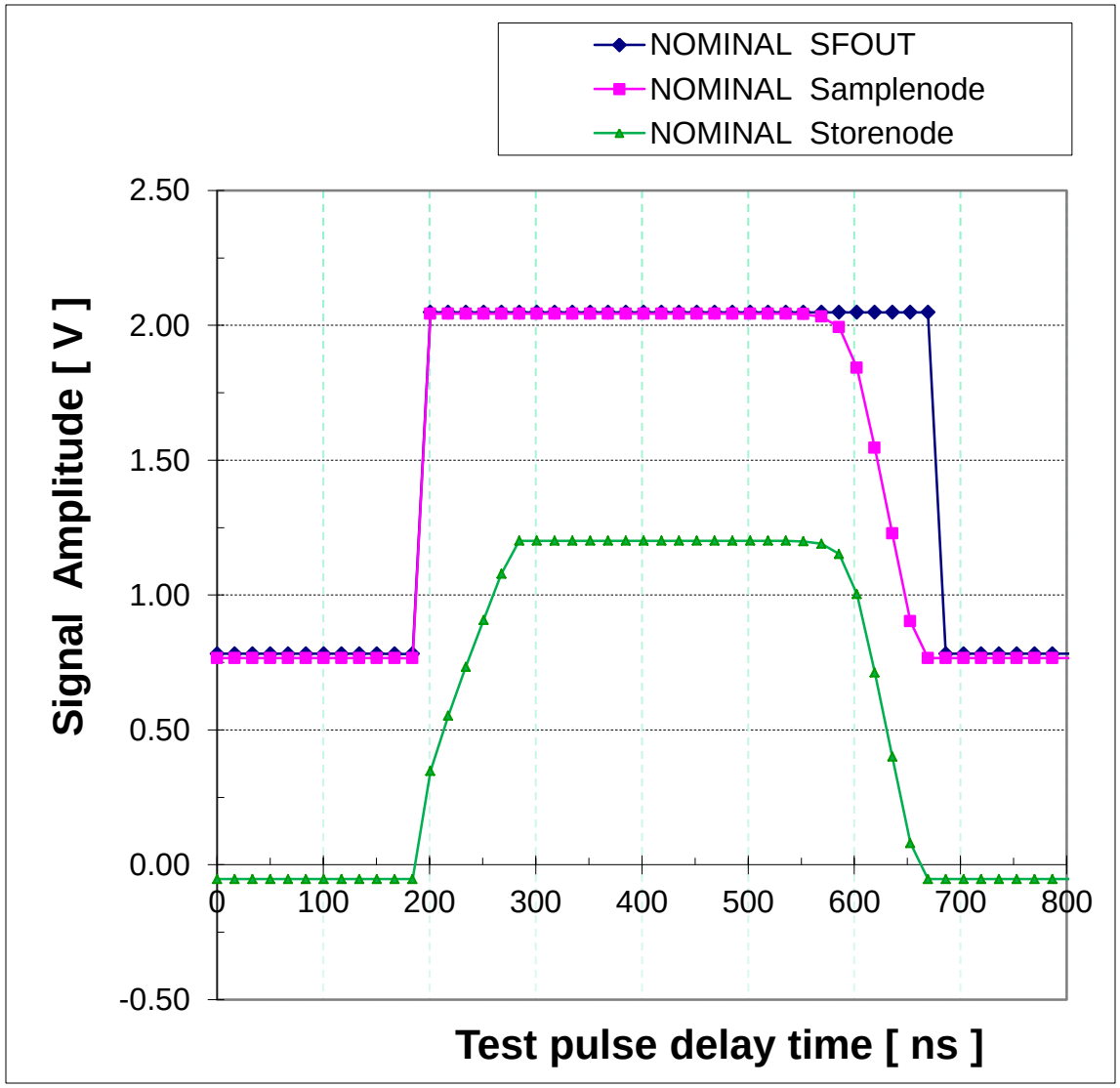
S. Lauxtermann, *Sensor Creations*, 2013-IIS Workshop

Photo-generated charge-carriers (e^-) are collected in Fast Drift Process at Front-Side (CMOS) Collection Junction

Summary

- pRAD-1 720×720-pixel 1st generation Rockwell Imager:
  - hybrid architecture: 26 μm pixels, SoC, QE~ 84%, < 180 min. int. time
  - 7 cameras in routine use (more on the way, reliably used over 8-years)
- 2nd generation pRAD-2 (Teledyne Imaging Sensors) hybrid imager prototype:
  - 40μm pixels, 1100×1100 px, lower read noise, 10-frame storage
  - large CMOS chip, low yield in CMOS and hybridization, high cost
- Commercial monolithic CMOS (front-illuminated) cameras issues with QE, fill factor and extinction ratio
- Back-side illuminated CMOS implemented in high resistivity Si, promising alternative to the hybrid architecture

PSpice simulations of pixel response 400ns gate



Response at nominal SF current: CDS ckt included in simulations, but not 100 µm detector. "Falling edge" is sample-node slew limited (large caps).